

INTRODUCTION

This application note has been compiled from a number of previously separate documents issued in response to specific customer requests for support or additional information about the operation and use of Mitel H.261 chips. As such the topics covered are included here under section headings which reflect the original document titles.

This application note should also be read in conjunction with the relevant IC datasheets and other H.261 applications notes. The latest versions of these can always be obtained from our Customer Service Centres but currently may be found in the October 1996 Media IC Handbook.

OPERATION OF THE VP520S WITH IMPERFECT SYNC INPUTS

Overview of the Problem

In the design of the VP520S, it was assumed that SYNC inputs conform exactly to the CCIR601 specification. However, in systems where certain video decoders such as the Brooktree Bt812 and Bt819 are used to extract VSYNC and HSYNC from the composite SYNC output of a camera, the extracted SYNCs do not conform exactly to the specification. In particular, the period of the HSYNC signal is not always 1728 SYSCCLKs (1716 SYSCCLKs in NTSC modes). It can vary by ± 1 clock. This uncertainty causes problems in the VP520S circuitry which interfaces with the external DRAM frame store - spurious or shortened RAS and CAS pulses may be output. In the NTSC modes problems will also be found in the circuitry which ensures correct alignment of output pictures.

A System - Level Solution

To avoid major modification of the VP520S, a system solution which relies on the use of an external FIFO has been implemented. A simplified block diagram of the relevant parts of the resulting system is given below. An NEC uPD485506 Line Buffer is recommended for the FIFO.

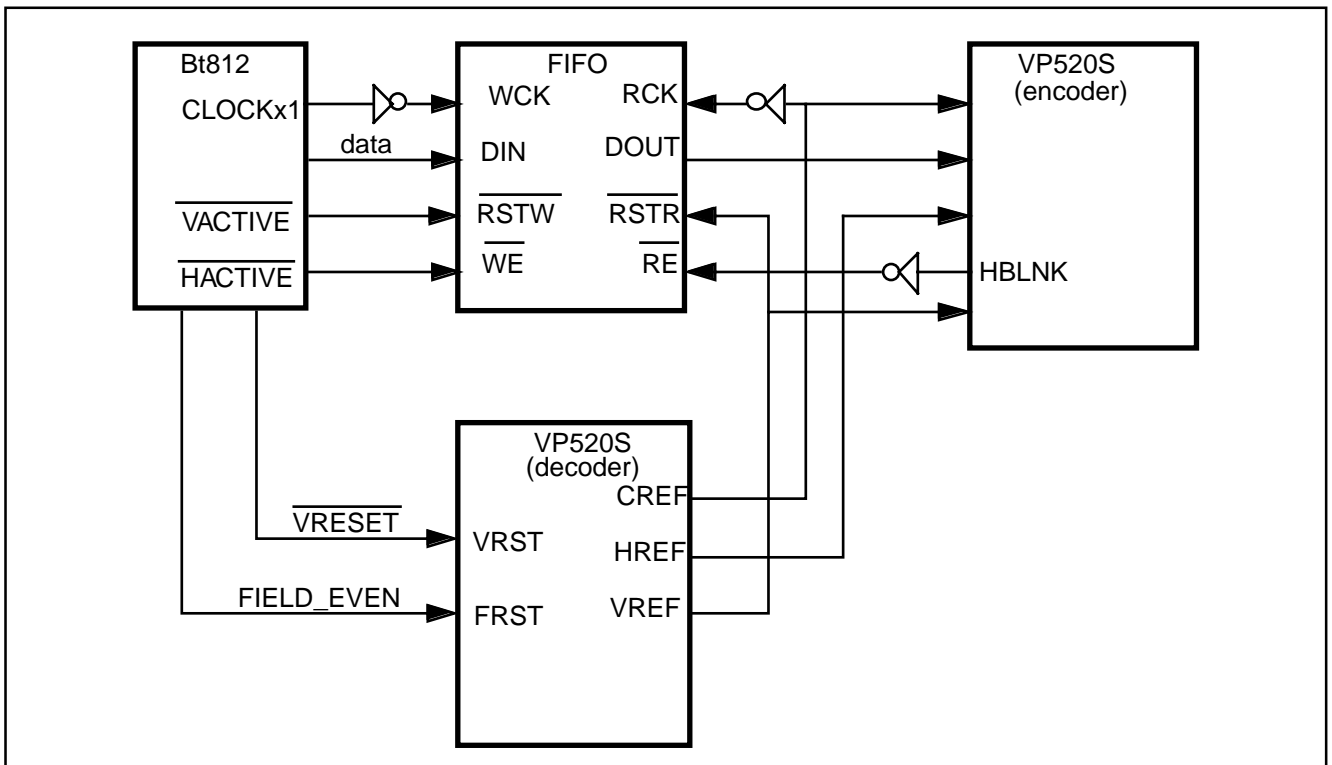


Fig. 1

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The FIFO has independent resets for the read and write addresses. The Bt812 resets the FIFO write address at the start of every video frame using the $\overline{\text{VACTIVE}}$ signal and strobes video data into the FIFO using its 13.5MHz clock. The FIFO read address is reset by the VP520S $\overline{\text{VREF}}$ and data is strobed out of the FIFO and into the encoder VP520S using the $\overline{\text{CREF}}$ from the decoder VP520S. Note also that $\overline{\text{HACTIVE}}$ and $\overline{\text{HBLNK}}$ are used as write and read enable signals respectively to ensure that only active data passes through the FIFO. This is necessary since the number of data words per line output by the Bt812 may vary.

To support this solution minor changes were made to the original VP520 design. To allow the first line of each frame to be correctly identified, $\overline{\text{VRESET}}$ and $\overline{\text{FIELD_EVEN}}$ signals from the Bt812 must be connected to the decoder VP520S $\overline{\text{VRST}}$ and $\overline{\text{FRST}}$ inputs respectively. These are used to reset the on chip SYNC generator at the start of each frame to keep it correctly aligned with the Bt812 SYNCs. The active edge of the $\overline{\text{VRST}}$ input is the falling edge. The first field of a frame is identified by the $\overline{\text{FRST}}$ input being LOW at the clock edge after the $\overline{\text{VSYNC}}$ falling edge.

Note that the SYNCs from the decoder VP520S will now not conform exactly to the CCIR601 specification. As the video camera and the Bt812 each have their own clock crystal, the number of clocks per frame will not be exactly 1728x625 (1716x525 for NTSC). If the number is greater than this, an extra HREF will be output at the end of the frame. If the number of clocks per frame is less than the ideal, the correct number of HREFs will be still be output.

The inaccuracy in the SYNCs output by the Bt812 arises because of the difference between the operating frequency of its clock and the frequency of the clock which drives the camera. Since both clocks will normally be produced by crystal oscillators with the same nominal frequency, a worst case assumption is that the two clocks will differ by at most 200ppm. This would give a maximum error of ± 216 in the number of clocks per frame (i.e. $\sim 0.02\%$). The solution described here will produce a jitter-free picture as long as, within a frame, the internal FIFO read address does not overtake the write address - or vice versa. This can be guaranteed if the absolute difference between the rising edges of $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ is at least 216 clocks and is less than the buffer length minus 216 clocks. It does not matter if the $\overline{\text{RSTR}}$ rising edge occurs first since the encoder VP520 can be programmed, via the line delay value, to ignore any invalid lines.

The on-chip SYNC generator will only be reset when there is a falling edge on $\overline{\text{VRST}}$ and $\overline{\text{FRST}}$ is LOW. However, to ease system proving, the mechanism can also be disabled via the host interface. To allow this, there is a further control register located at host address 3. Details of its programming are given in the VP520S (DS3504 - 3.2) datasheet.

FLOW CHART AND SAMPLE CODE FOR H.261 BUFFER CONTROL

A simple buffer control strategy has been developed to support the VPB261 H.261 Evaluation Board. The code for this is supplied as part of the driver software which ships with the board and is also detailed in the associated User Guide. The flow chart below is supplied to allow a more ready appreciation for the operation of buffer control and for completeness the source code is also reproduced here.

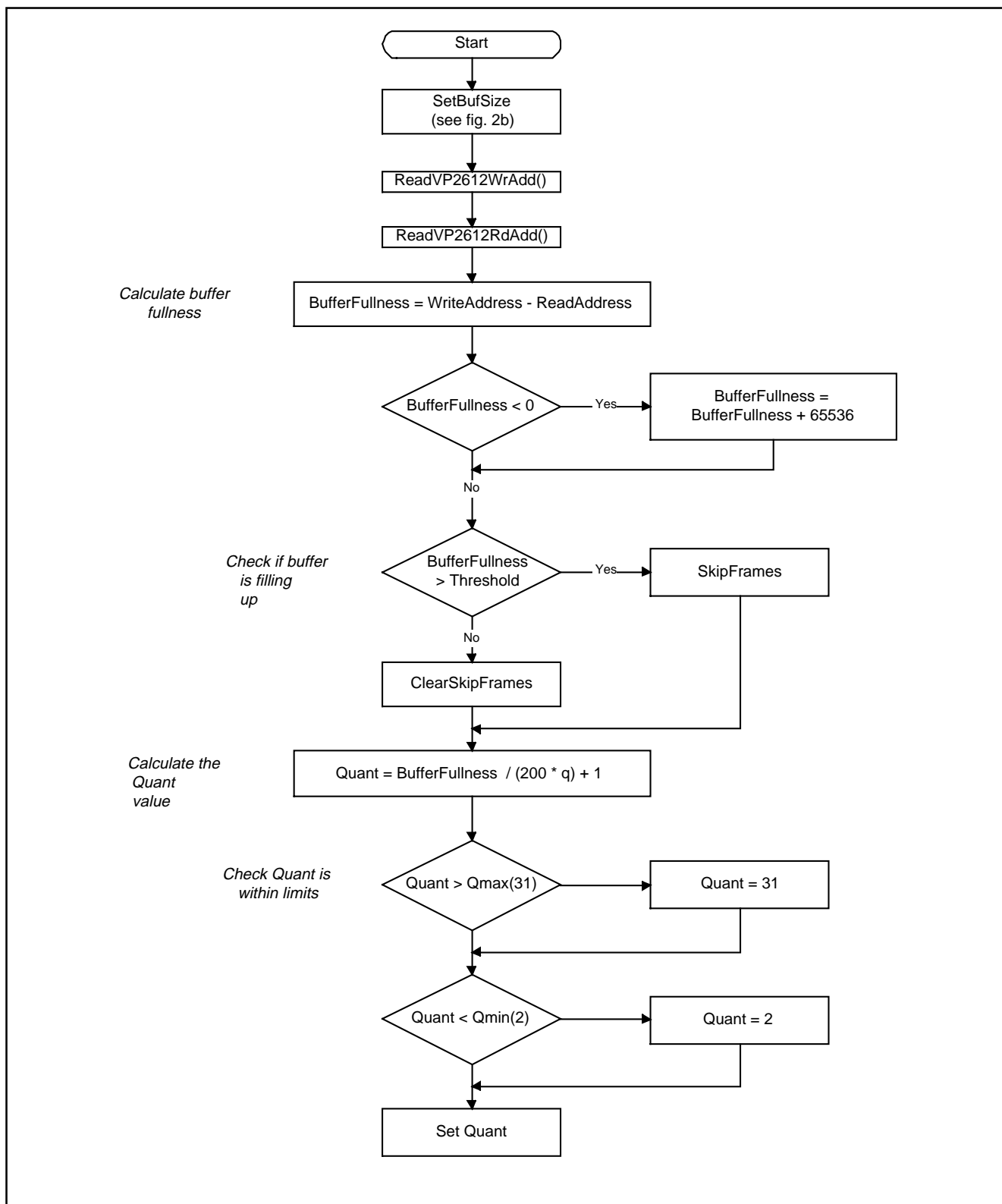


Fig. 2a H.261 Buffer control algorithm

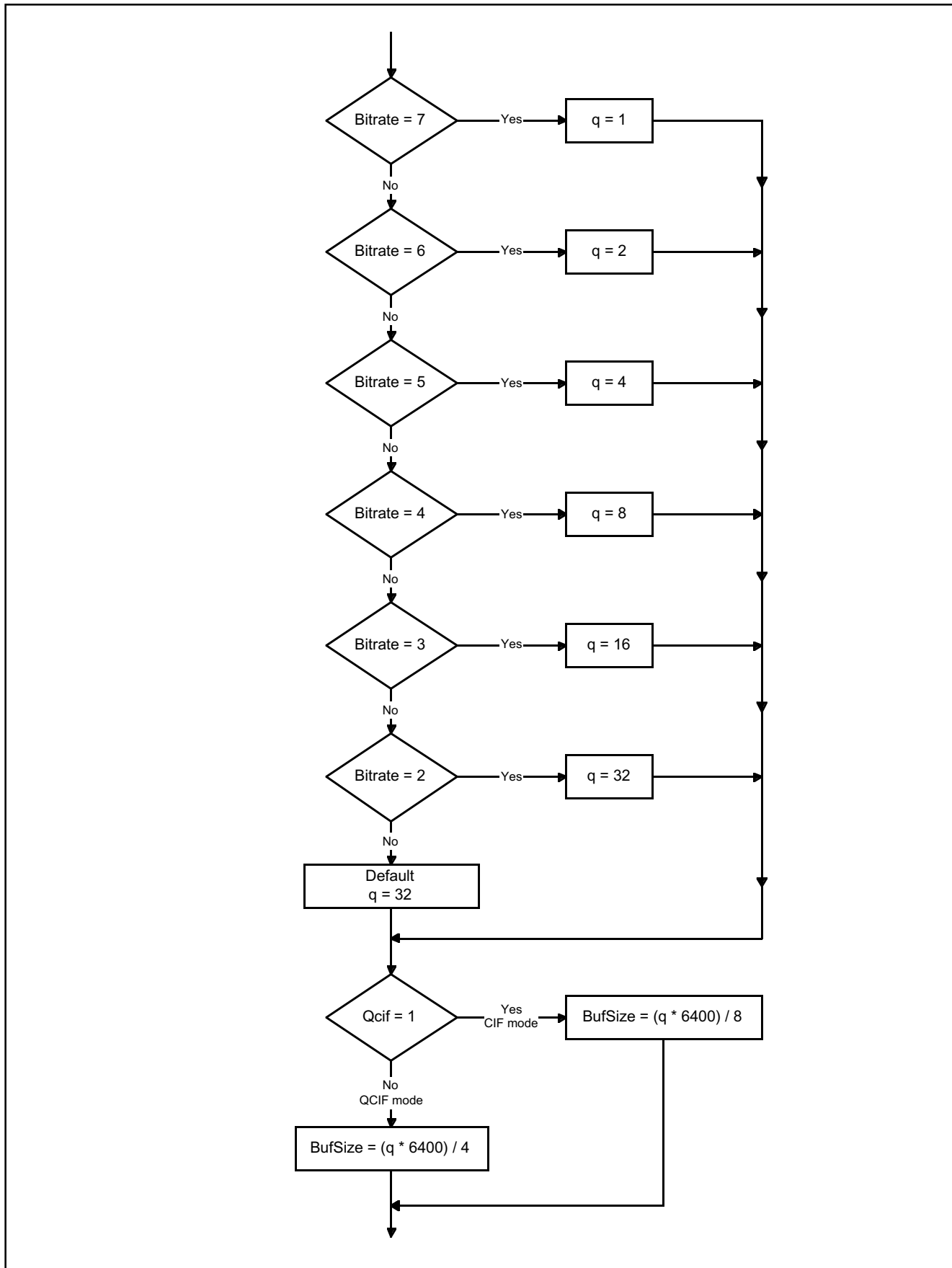


Fig. 2b Set Buffer Size

Bit Rate	Buffer size in bytes	
	CIF	QCIF
64kb/s	1.6k	0.8k
128kb/s	3.2k	1.6k
256kb/s	6.4k	3.2k
512kb/s	12.8k	6.4k
1Mb/s	25.6k	12.8k
2Mb/s	51.2k	25.6k

Table 1. Buffer sizes for a given bit rate

RM8 BUFFER CONTROL, 'C' SOURCE CODE:

```
#define VP2611_SkipFrames    64        //set skip frame bit
#define VP2611_ClearSkipFrames 0      //reset skip frame bit
```

//write a byte to the VPB261

```
void write_bd(int device,int address,int data)
{
    outportb(AddrReg, address);
    outportb(device, data);
}
```

void ReadVP2612WrAdd(void)

```
{
    outportb(AddrReg, 8);
    WriteAddress = inportb(VP2612);
    outportb(AddrReg, 9);
    WriteAddress = (WriteAddress * 256) + inportb(VP2612);
}
```

void ReadVP2612RdAdd(void)

```
{
    outportb(AddrReg, 10);
    ReadAddress = inportb(VP2612);
    outportb(AddrReg, 11);
    ReadAddress = (ReadAddress * 256) + inportb(VP2612);
}
```

void SkipFrames(void)

```
{
    //start skipping frames
    write_bd (VP2611, 0, 5);
    write_bd (VP2611, 1, VP2611_SkipFrames);
}
```

void ClearSkipFrames(void)

```
{
    //stop skipping frames
    write_bd (VP2611, 0, 5);
    write_bd (VP2611, 1, VP2611_ClearSkipFrames);
}
```

void SetQuant(void)

```
{
    write_bd(VP2611, 0, 2);
    write_bd(VP2611, 1, Quant);
}
```

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```
void FAR PASCAL _export buf_control (int Bitrate, int Qcif, int Qmin,
                                     int Qmax, int Threshold,
                                     LPTRDATASTRUCT lptrDataStruct) {

    BufferFullness = 0;

// SetBufSize
    switch (Bitrate) {
        case 7: q = 1; break;
        case 6: q = 2; break;
        case 5: q = 4; break;
        case 4: q = 8; break;
        case 3: q = 16; break;
        case 2: q = 32; break;
        default: q = 32;
    }
    if (Qcif) BufSize = ((q * 6400) / 8); //divide by 8 for No. of bytes
    else BufSize = ((q * 6400) / 4); //buffer sizes are doubled for CIF

//read buffer read/write pointers
    ReadVP2612WrAdd();
    ReadVP2612RdAdd();
//calculate buffer fullness
    BufferFullness = WriteAddress - ReadAddress;
//check for buffer under-flow
    if (BufferFullness < 0) BufferFullness = BufferFullness + 65536;

//BufferControl
//check if buffer is filling up
    if (BufferFullness > (BufSize * Threshold) / 100)
        SkipFrames();
    else ClearSkipFrames();

//calculate the Quant value
    Quant = (BufferFullness / (200 * q)) + 1;
//check Quant is within limits
    if (Quant > Qmax)
        Quant = Qmax;
    if (Quant < Qmin)
        Quant = Qmin;
//update Quant value
    SetQuant();
}
```

UNDERSTANDING AND DETERMINING FILTER COEFFICIENTS FOR THE VP520S

The following text offers a brief description of the scaling and filtering operations provided by the VP520S PAL/NTSC to CIF/QCIF Converter. In particular it attempts to explain the effects of different filter coefficients on the resulting performance of the device.

Encoder Filtering

In CIF encoder mode, the horizontal filter block reduces the number of pixels per line from 720 to 352, i.e. it essentially halves the horizontal resolution of the picture. One way of generating the output pixels could be to average successive pairs of the input pixels. This operation can be considered as a filtering operation with the following transfer function, where the X axis value is in multiples of the input pixel spacing.

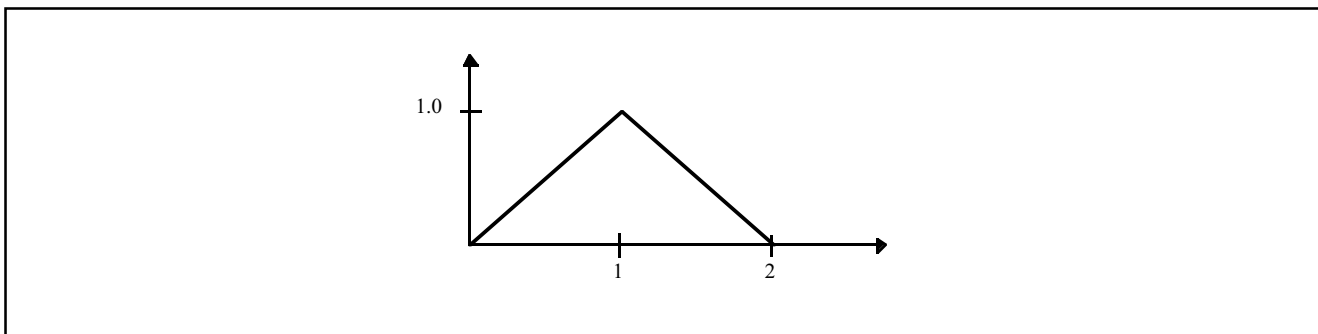


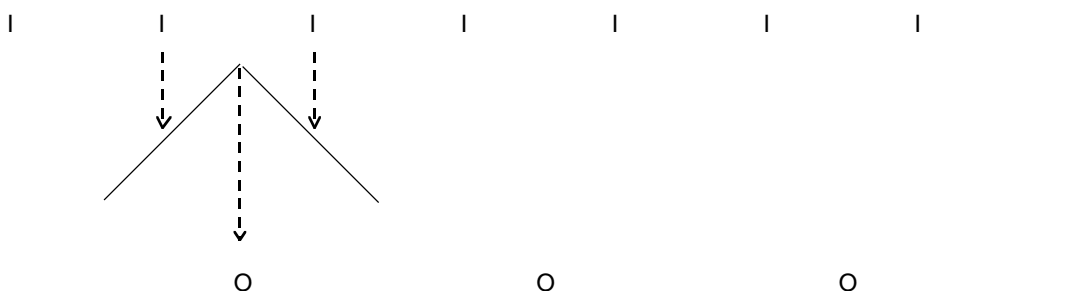
Fig. 4

If the position of the output pixels is to be half way between the corresponding inputs, the transfer function should also be considered as being centred half way between the inputs. The transfer function is then sampled at the input pixel positions to obtain the filter coefficients. In this case, two filter coefficients of value 0.5 are obtained and the output is therefore the average of two input pixel values.

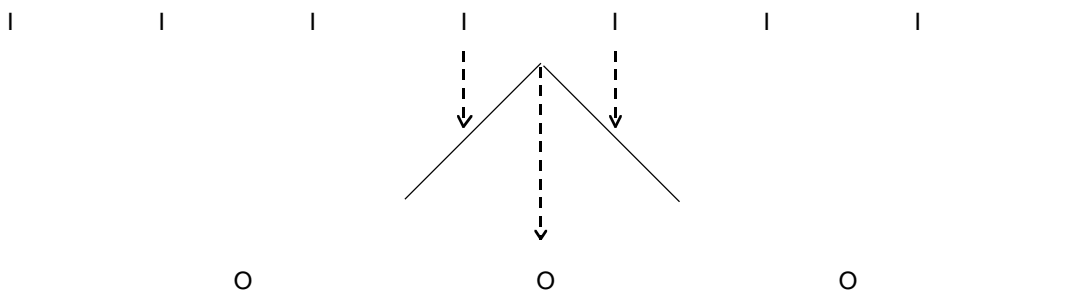
The diagrams on the next page illustrate this and show how a sequence of three output pixels would be calculated. In the diagrams, the 'I' characters represent the positions of the input pixels and the 'O' characters are output pixel positions.

Note that in all of the following descriptions it is assumed that unused filter coefficients are set to zero.

1st pixel

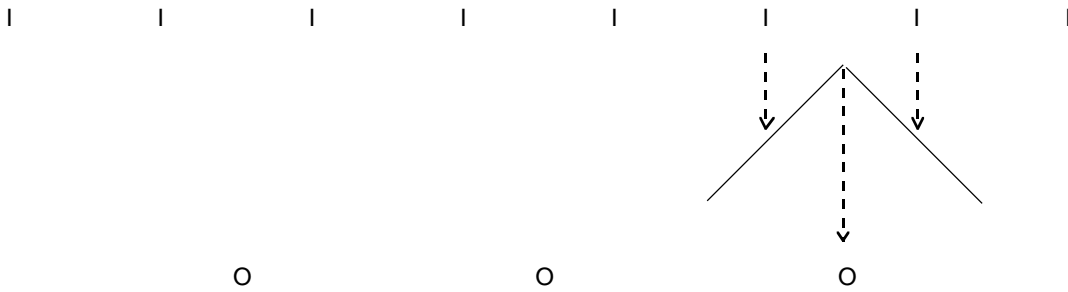


2nd pixel

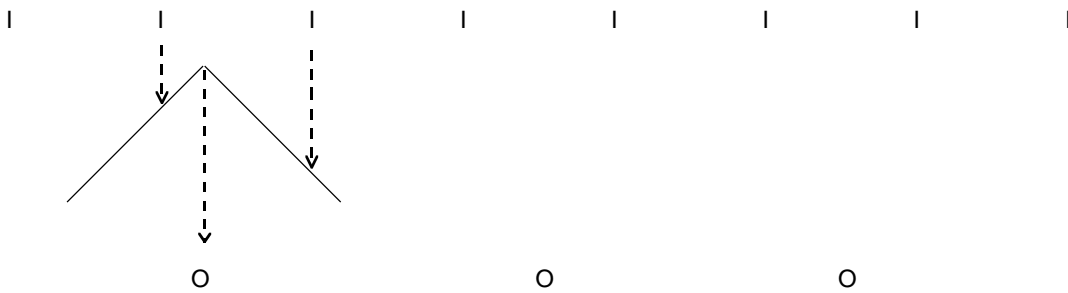


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3rd pixel

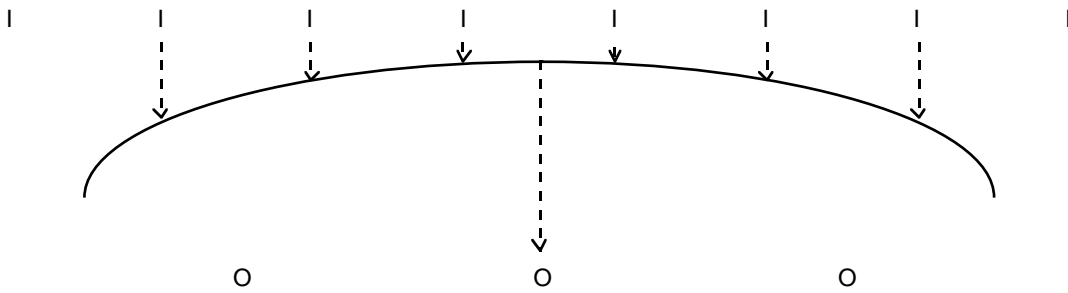


Suppose now that it is required to position the outputs closer to the first of the pair of inputs. This is done by centering the transfer function at the new position and sampling to get the new filter coefficients. Thus, to position the outputs one quarter pixel after the first input, the coefficients would be 3/4 and 1/4 as shown below.



To simply sample every alternate input to produce the output pixels, the transfer function can be shifted further to the left until it is in line with the first input pixel of the pair. This would then give coefficients of (1,0). Shifting to the right to get coefficients (0,1) is equivalent to selecting the second pixel of each pair.

Since the horizontal filter has 8 taps in CIF encoder mode, it is possible to implement more complex filters than that described above. For example, the coefficients of a 6 tap filter could be calculated using a diagram of the following type.

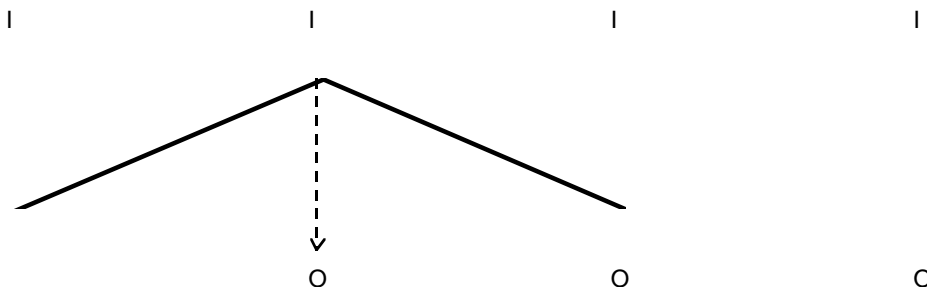


In encoder modes, it is usual to construct a low pass filter to remove noise and to avoid aliasing in decoded pictures. To completely avoid aliasing it is necessary to choose a filter with a cut-off frequency which is less than or equal to half the sampling frequency of the output data. Therefore for the horizontal luminance filter in CIF encoder mode, the ideal filter would have a cut-off frequency of 3.375MHz. The chrominance filter cut-off should be half of this. In QCIF modes these cut-off frequencies would be halved again. Note however that the high degree of smoothing implied by ideal filters may give an unacceptably blurred image. Experimentation with different cut-off frequencies may be required to arrive at the best compromise between picture sharpness and the presence of aliasing artifacts.

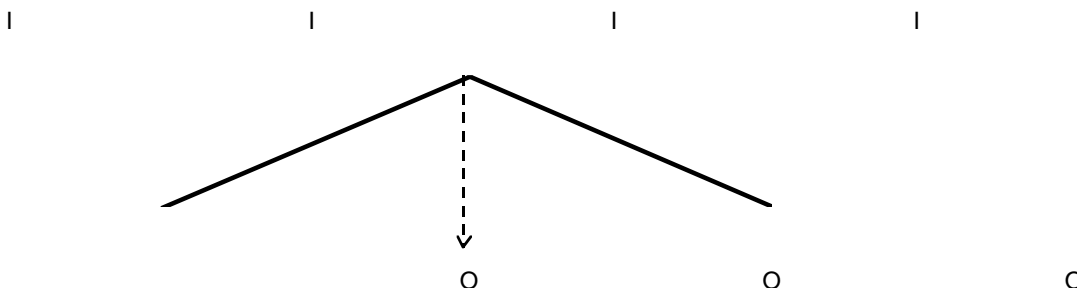
Decoder Filtering

In the decoder modes the filters increase the number of pixels by interpolation. Thus in CIF decoder mode the horizontal filter essentially doubles the number of pixels per line - for every input pixel, two pixels are output. To allow the equation for each of the pair of output pixels to be different, the horizontal filter has two sets of coefficients. In the simplest setup, the two sets are identical and the output line is produced by generating two identical pixels for every input pixel. A simple extension to this could involve two transfer functions. The first causes the output pixel to be identical to the input value. The second outputs a value which is the average of adjacent input values. These transfer functions are shown below.

1st transfer function - coefficients = (1,0)



2nd transfer function - coefficients = (0.5,0.5)



The coefficients above are expressed as decimals. However, within the VP520S they are stored as 8 bit two's complement numbers. The most positive value, 127, represents the fraction 127/128. The most negative value, -128, represents -128/128 (i.e. -1). To ensure that a filter has a gain of 1, the sum of its binary coefficients should equal 128. Note that where only a single non-zero coefficient is used, the gain can be no bigger than 127/128.

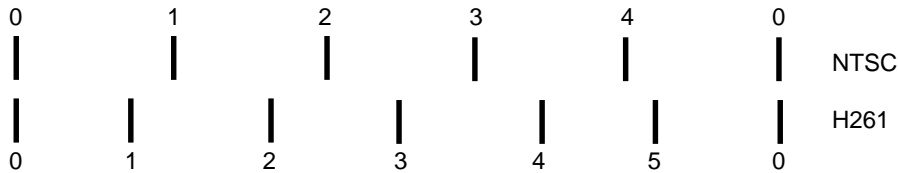
Apart from the NTSC CIF modes, the principles of operation of the vertical filter are similar to those of the horizontal filter. However, in the decoder modes, the two video fields have different sets of coefficients. This allows accurate spatial positioning of the output data by centering the filter transfer functions differently for each field.

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NTSC Mode

The CIF NTSC modes are different due to their more complex scaling requirements. In encoder modes only one of the two video fields is encoded to produce the H261 image. Since an H261 CIF image has 288 lines and an NTSC video field has 240 active lines, it is necessary to scale the video image vertically by a factor of 6/5 during the encoding process. Similarly, when decoding, it is necessary to vertically scale the H261 image by 5/6. In some systems, this scaling is achieved crudely by repeating every 5th line when encoding and discarding every 6th line when decoding. However, in the VP520S, the H261 images are processed in groups of 6 lines with a different set of coefficients for each of the six. This allows accurate scaling to be achieved.

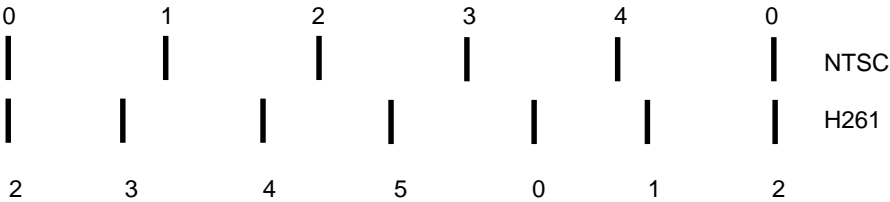
To simplify the explanation of the scaling process, only the simple linear filter transfer function described above will be covered here. However, as long as they are centred in the same way, more complex transfer functions can be used.



The above diagram shows the position of a set of 5 NTSC lines relative to the associated H261 lines. Using the two coefficient filter described above, the first two output lines (0 and 1) are formed from input lines 0 and 1. Output lines 2 to 5 are formed from input lines 1 and 2, 2 and 3, 3 and 4, 4 and 0 respectively. Thus for this example the 6 coefficient sets would be (1,0), (1/6,5/6), (2/6,4/6), (3/6,3/6), (4/6,2/6), (5/6,1/6).

The above diagram also applies to the generation of the first field of the NTSC frame in decoder mode. NTSC output lines 0 to 4 are formed from H261 input lines 0 and 1, 1 and 2, 2 and 3, 3 and 4, 4 and 5 respectively. Internally, the vertical filter also produces an output from H261 lines 5 and 0 but this is discarded. There are therefore 6 sets of coefficient pairs with values (1,0), (4/5,1/5), (3/5,2/5), (2/5,3/5), (1/5,2/5) and (don't care, don't care).

For the second field in NTSC CIF decoder mode the diagram below applies. The H261 line sequence is shifted by two positions to the left. This results in the output formed from H261 lines 1 and 2 being discarded. For the simple filter the coefficient pairs are therefore (1/5,4/5), (don't care, don't care), (1,0), (4/5,1/5), (3/5,2/5) and (2/5,3/5).





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